Department of Mathematics, University of Padua

Ravenscar-EDF

Comparative Benchmarking of an EDF Variant of a Ravenscar Runtime

Ada Europe 2017
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Outline of the Talk

- **1973**: Liu and Layland address the question of which online (preemptive) scheduling policy for single-core processors is theoretically the best

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- **2005**: Buttazzo sustains the superiority of EDF also from a practical standpoint
- **2017**: We present an empirical, quantitative comparison between concrete implementations of EDF and FPS

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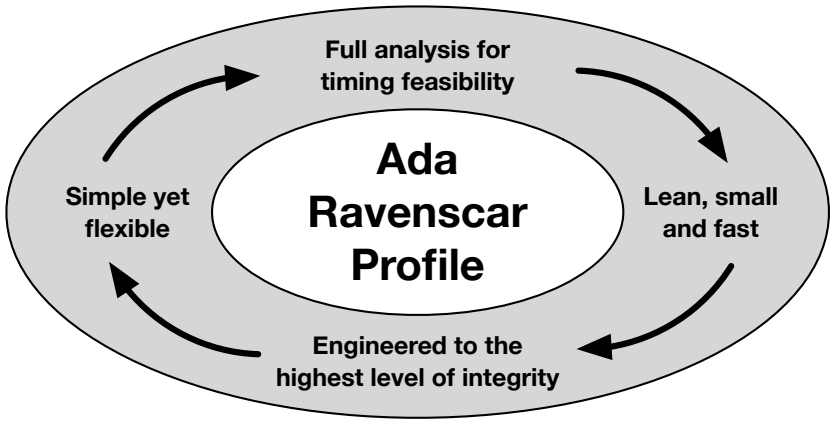
3. We stressed each system to the theoretical limit discussed in the literature
   - Using exactly the same, unchanged, application software
   - The switch of scheduling policy is completely transparent to it

- The Ravenscar profile is an important asset of the Ada programming language



The RM-to-EDF Transformation Process

The Ada Ravenscar Profile

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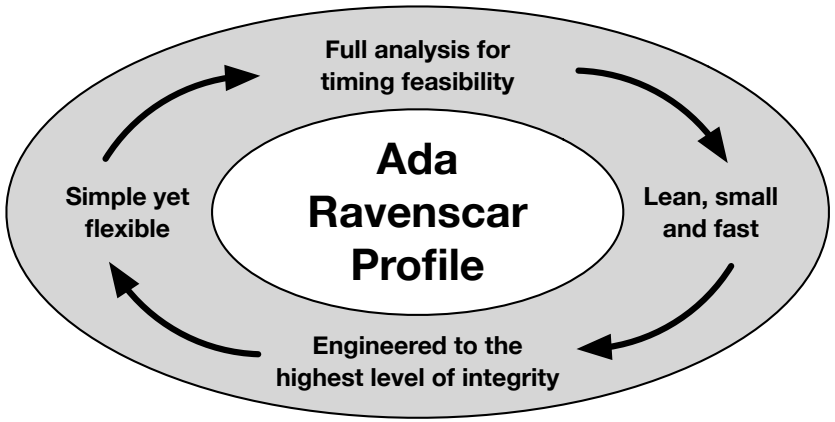

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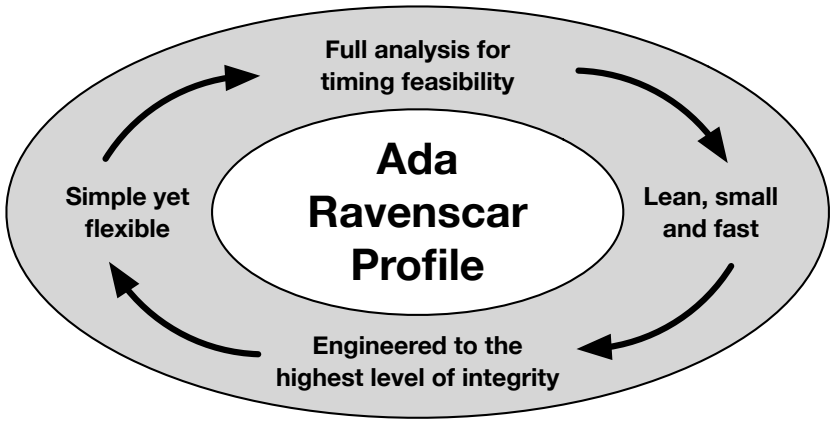
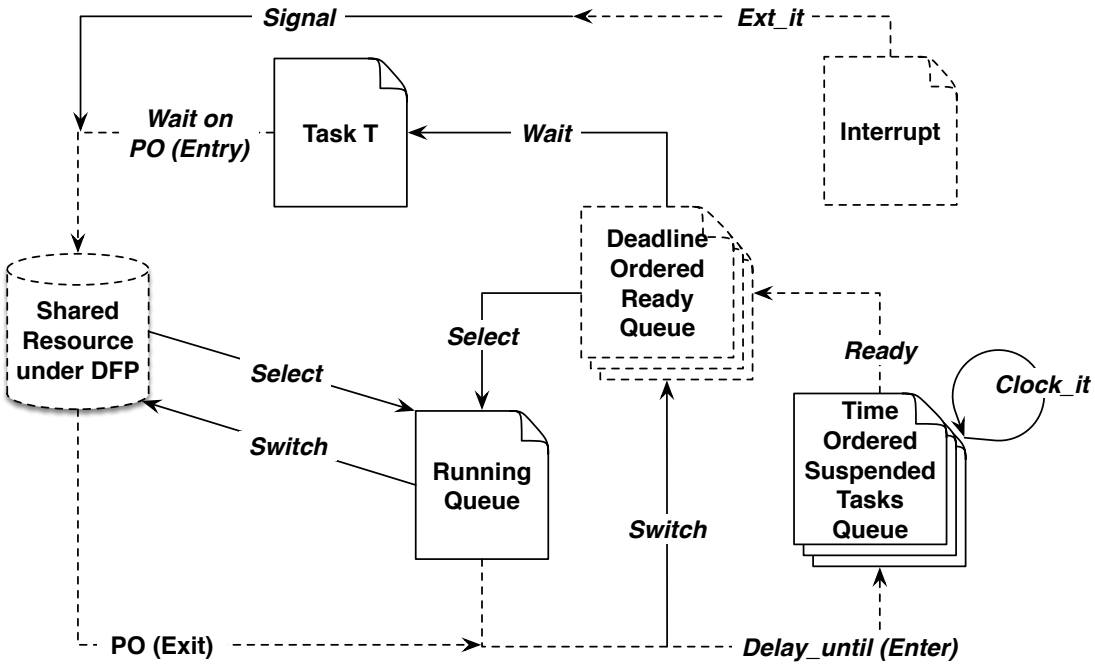


- The first-ever Ravenscar runtime to be released for industrial use was produced by AdaCore for the LEON processor family
- That technology originated from a fork of the Open Ravenscar Real-Time Kernel (ORK+) developed by the Technical University of Madrid for the European Space Agency (ca. 2000)

The RM-to-EDF Transformation Process

Turning Priorities into Deadlines



1. **Task Dispatching Policy**: from *"FIFO Within Priorities"* to *"EDF"*[1]
2. **Locking Policy**: from IPCP to DFP[2]

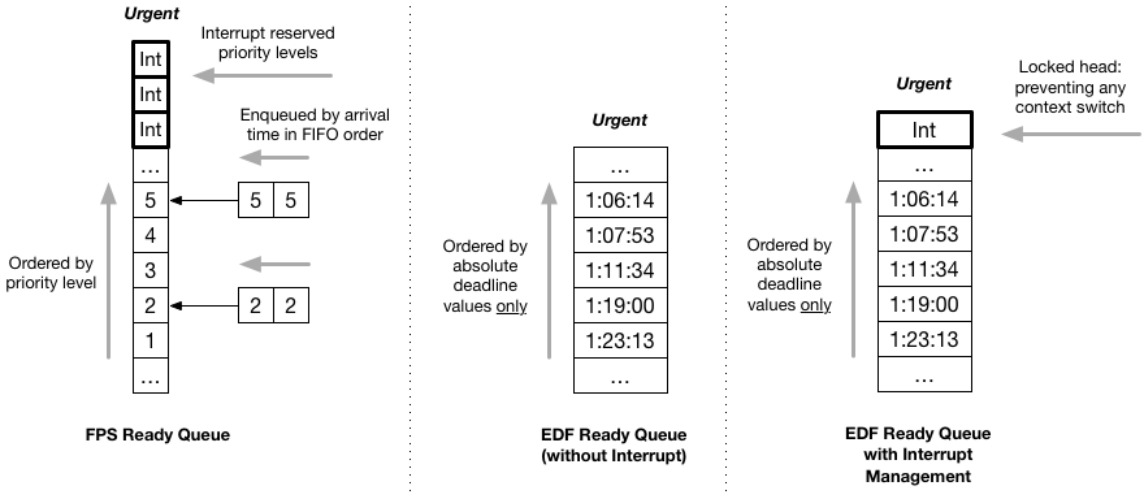
[1] A. Burns, An EDF Runtime Profile based on Ravenscar. Ada Lett. 33, 1 (June 2013)

[2] A. Burns and A. Wellings. The Deadline Floor Protocol and Ada. Ada Lett. 36, 1 (July 2016)

The RM-to-EDF Transformation Process

Implementation Challenges

Interrupt handling intrinsically assumes priorities, which – in principle – do not belong in an EDF system



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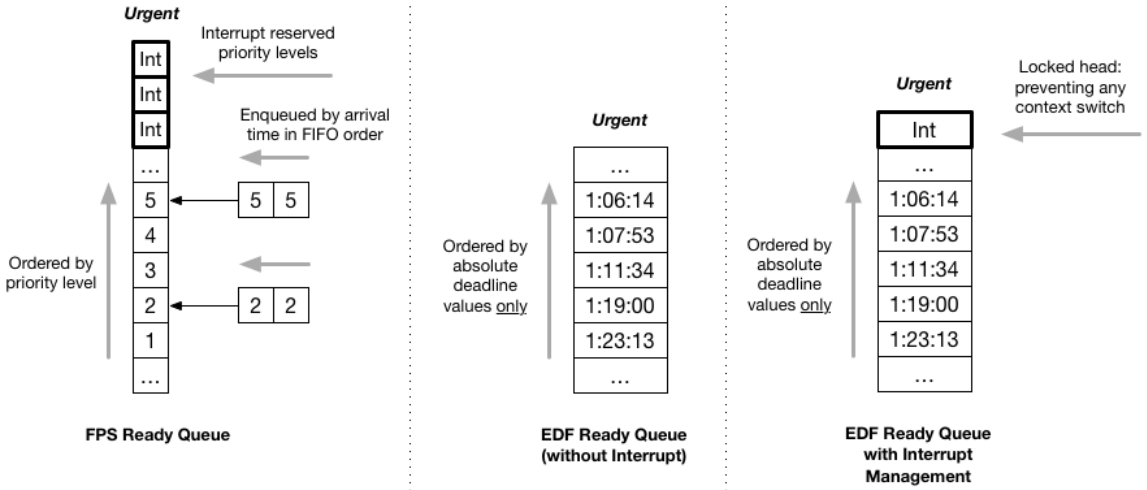

- Our solution reserves a fictitious position at the top of the ready queue for the current interrupt handler
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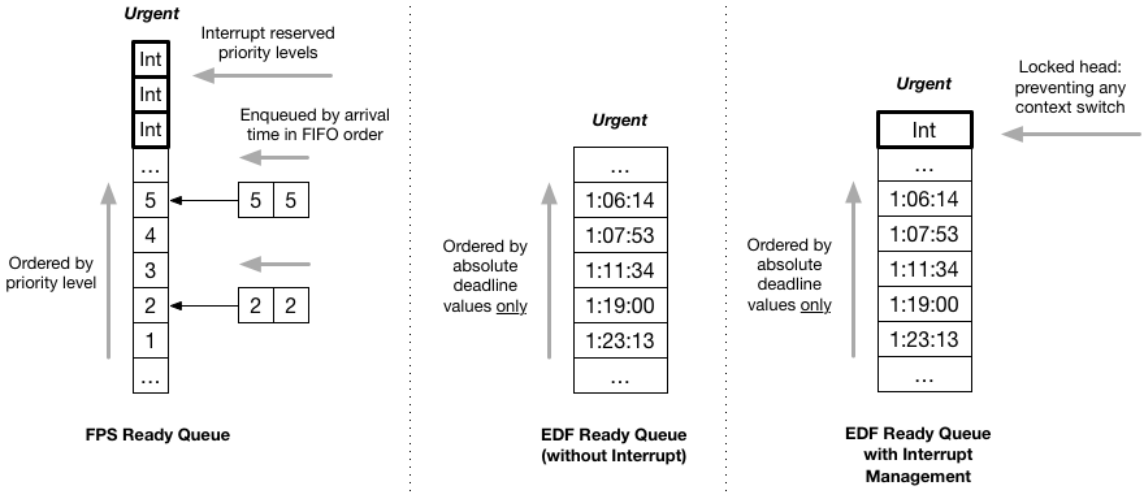
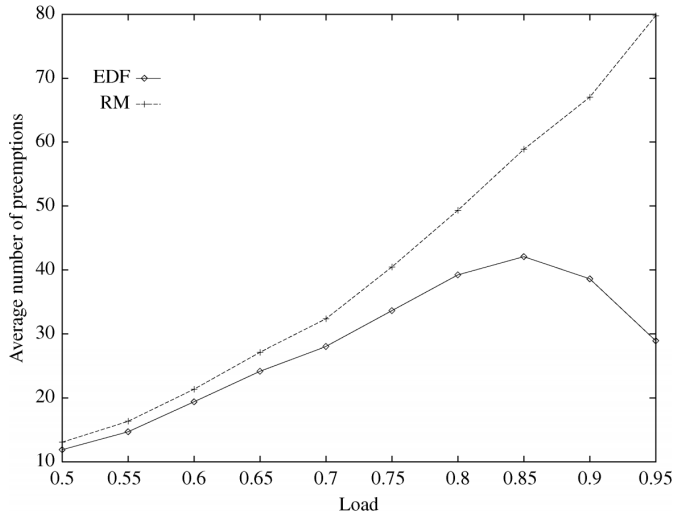


- Our solution reserves a fictitious position at the top of the ready queue for the current interrupt handler
  - If an interrupt handler is active, that position is used and the deadline-based part of the queue is frozen
  - If no interrupt is running, that position is not in use and cannot be contended

Buttazzo claimed EDF better than RM (FPS) in many respects

- Lower runtime overhead
  - Less preemptions
- Easier analysis
- More robust under overloads
  - Transient
  - Permanent



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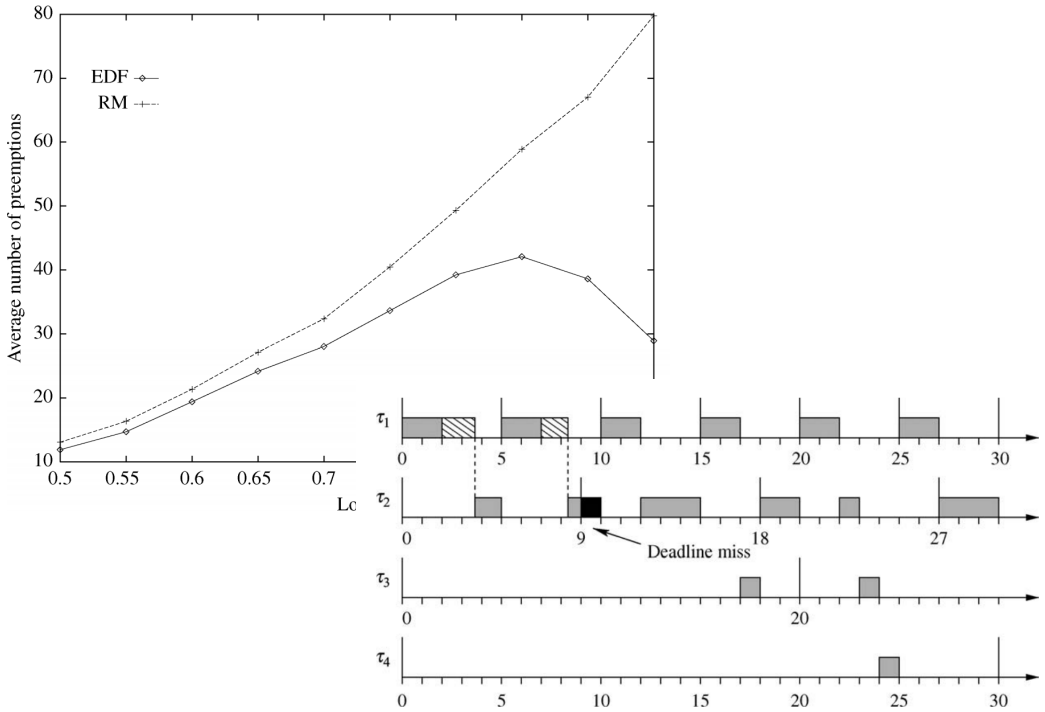

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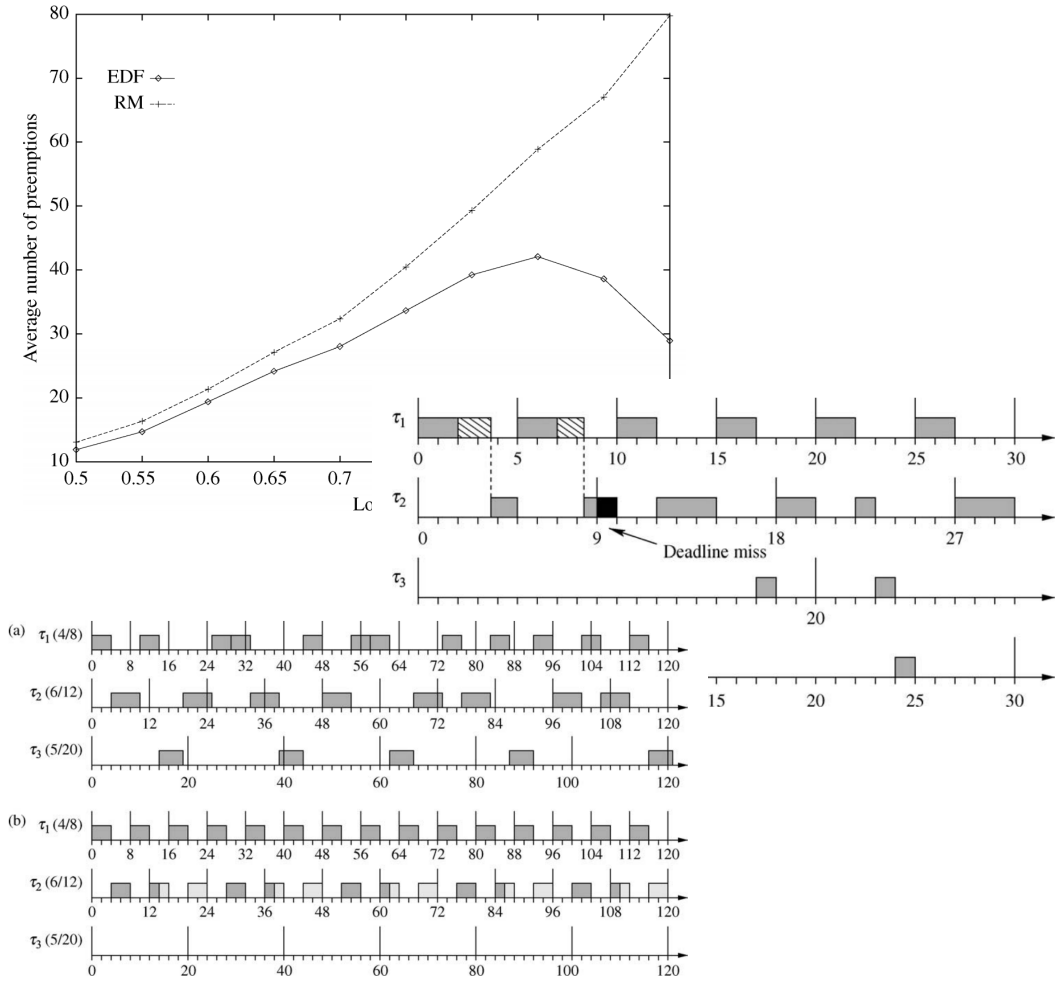

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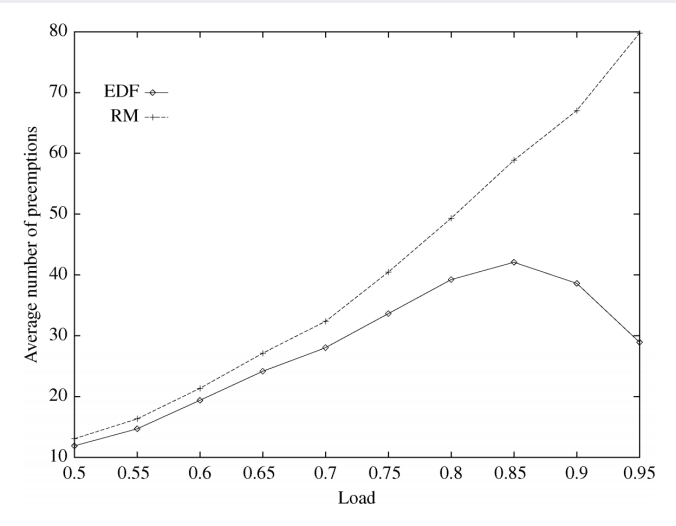

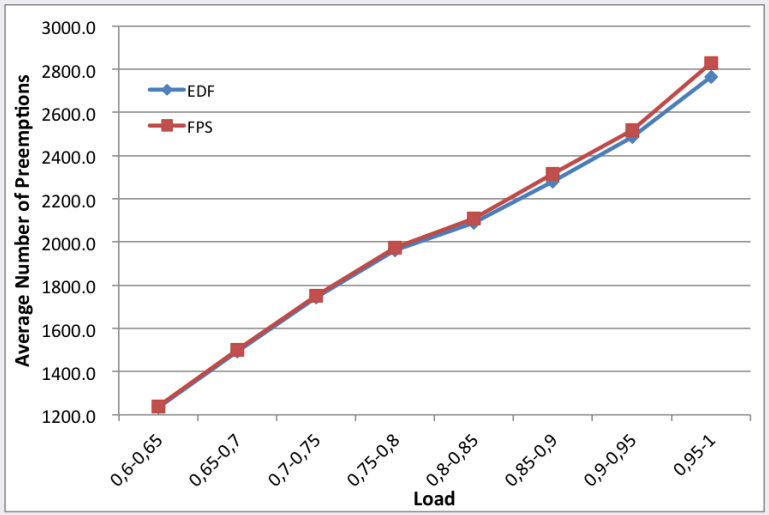

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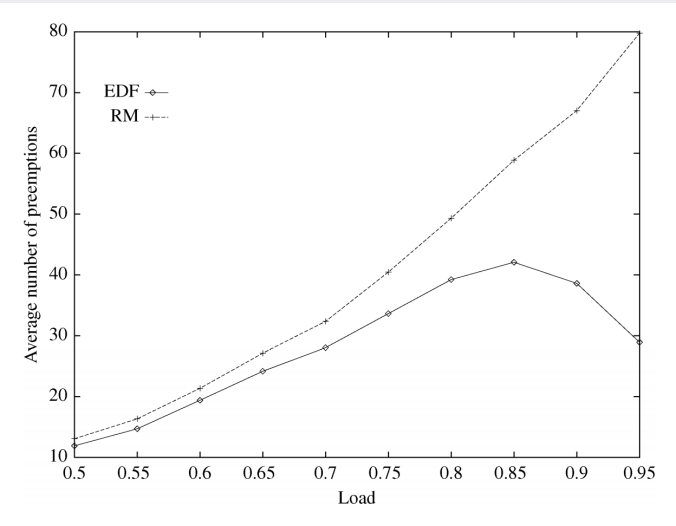

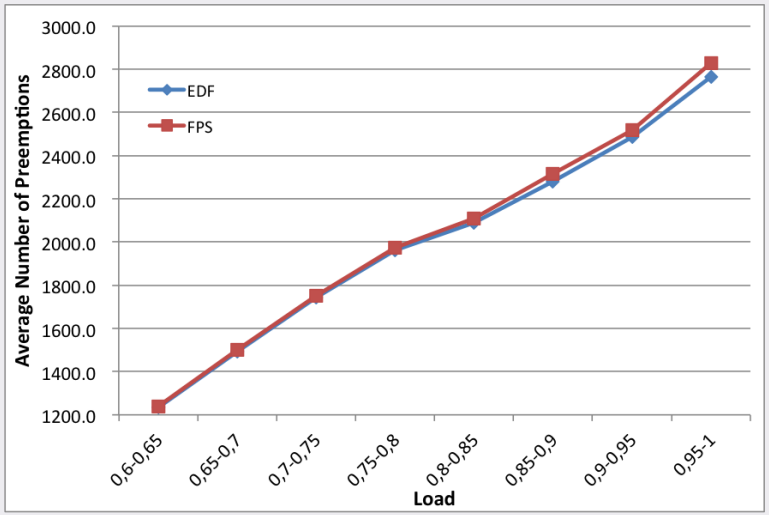

- Lack of practical implementation and analysis of resource sharing protocols

Evaluation Results
Highest Schedulable Utilization

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Taskset Type	Task Types	Delta Schedulable Utilization	Max CPU Load	EDF			FPS		
				RC	DM	PR	RC	DM	PR
Constrained	Short & Mid	**2,89%**	105,50%	30.714	0	3.637	29.850	415	6.202
Implicit	Mid Only	**3,72%**	102,63%	18.691	0	837	18.021	673	2.040
Constrained	All	**0,05%**	104,06%	24.398	0	5.131	24.409	0	5.211
Implicit	All	**5,22%**	100,85%	24.935	953	6.309	26.236	0	5.715

- **RC**: count of regular completions
- **DM**: count of deadline misses
- **PR**: count of preemptions

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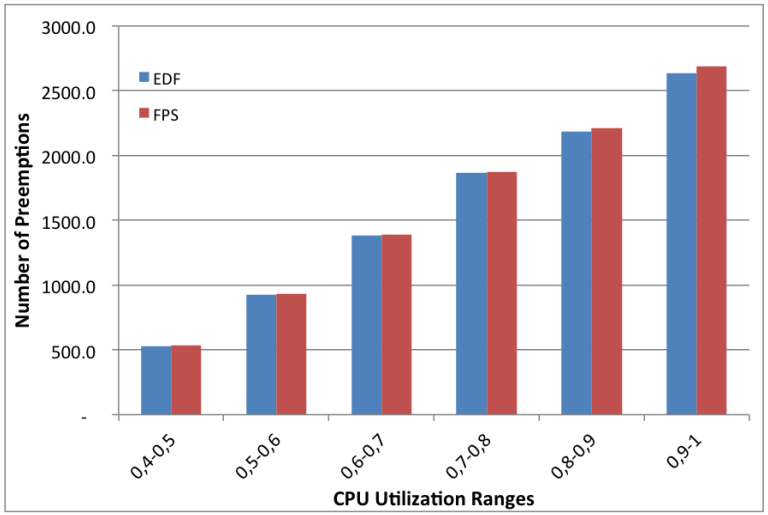

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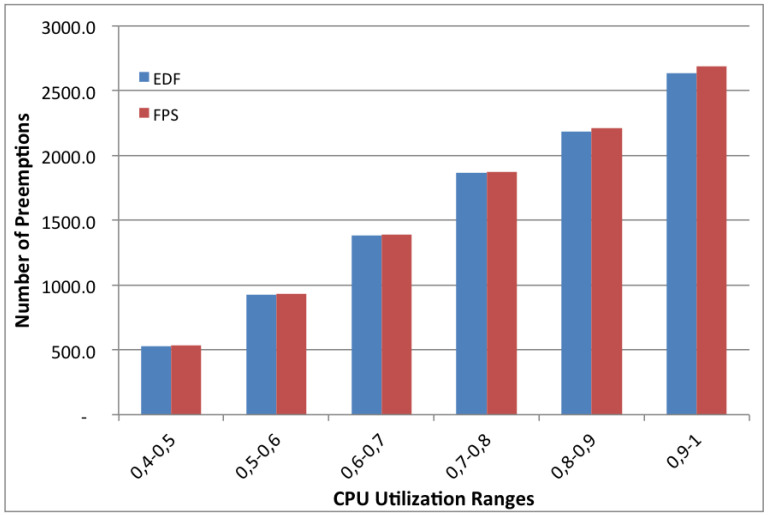

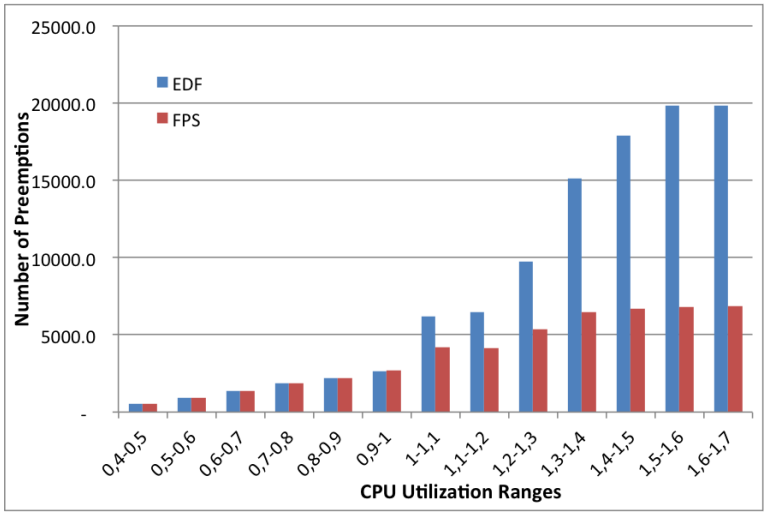

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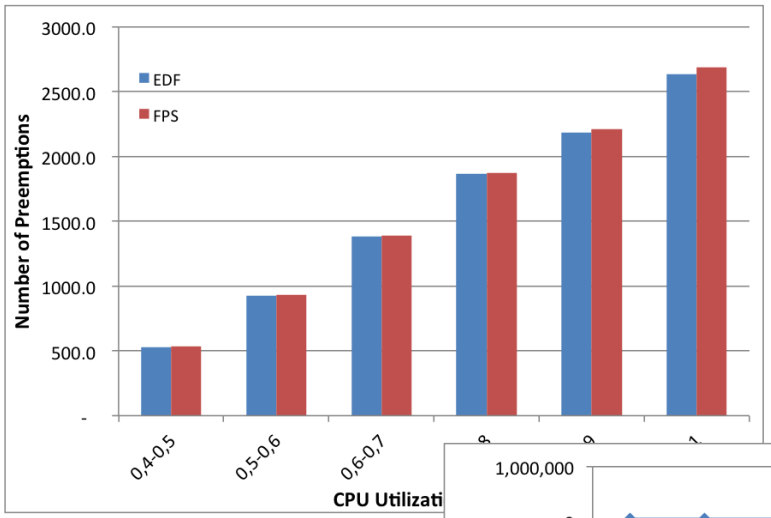

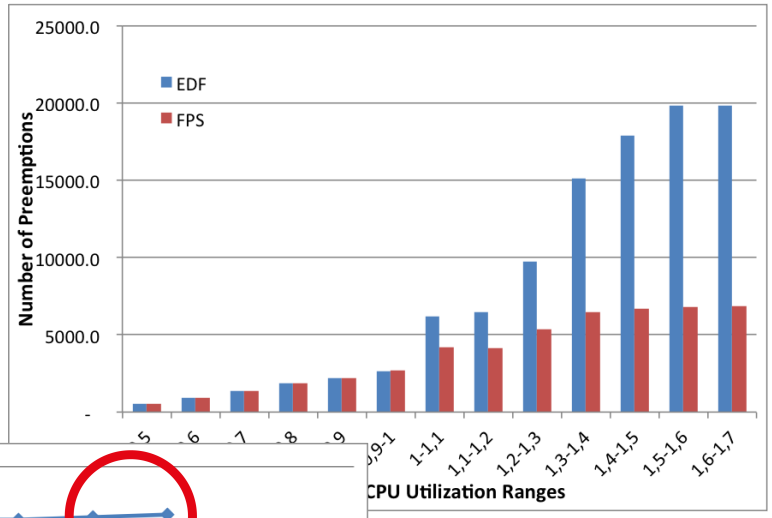

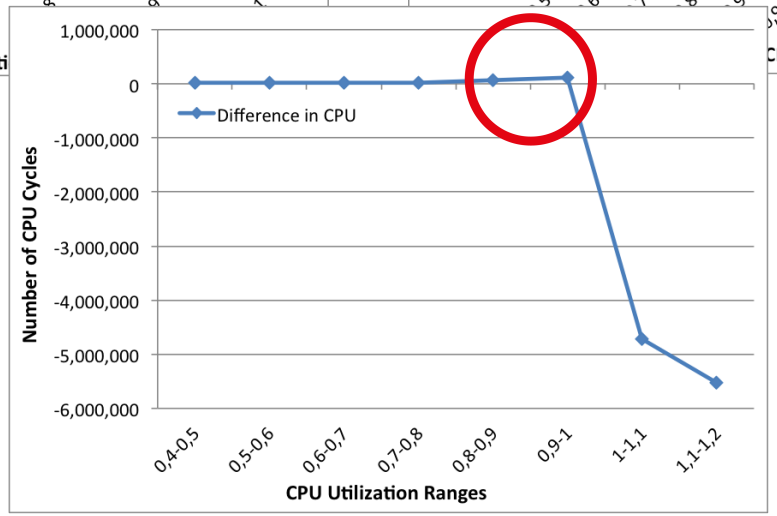

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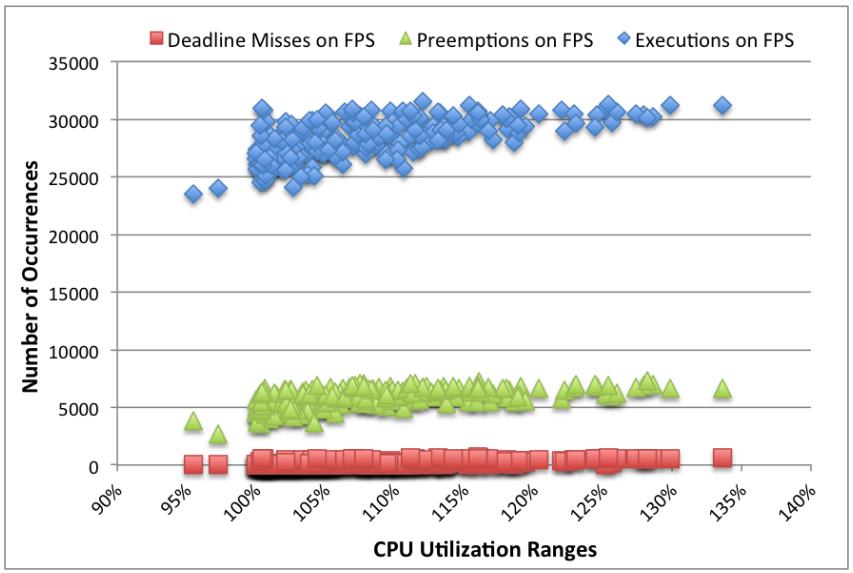

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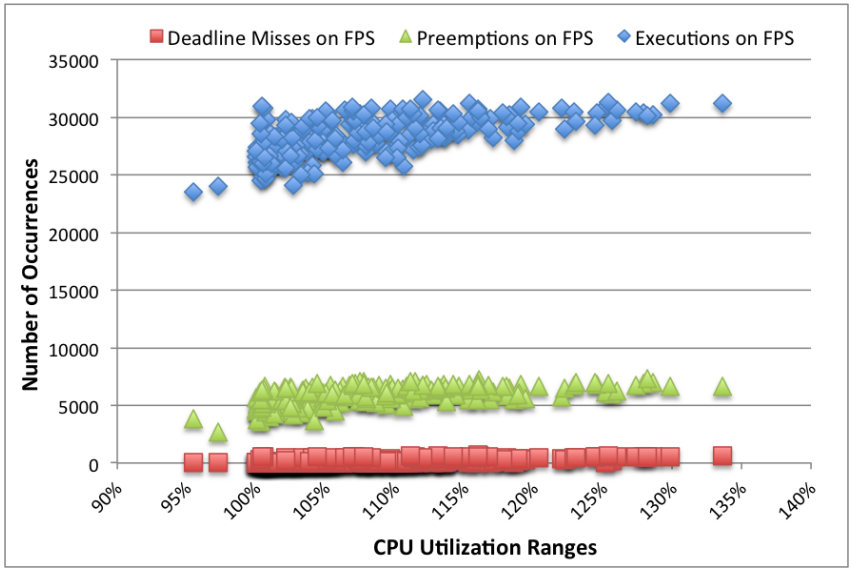

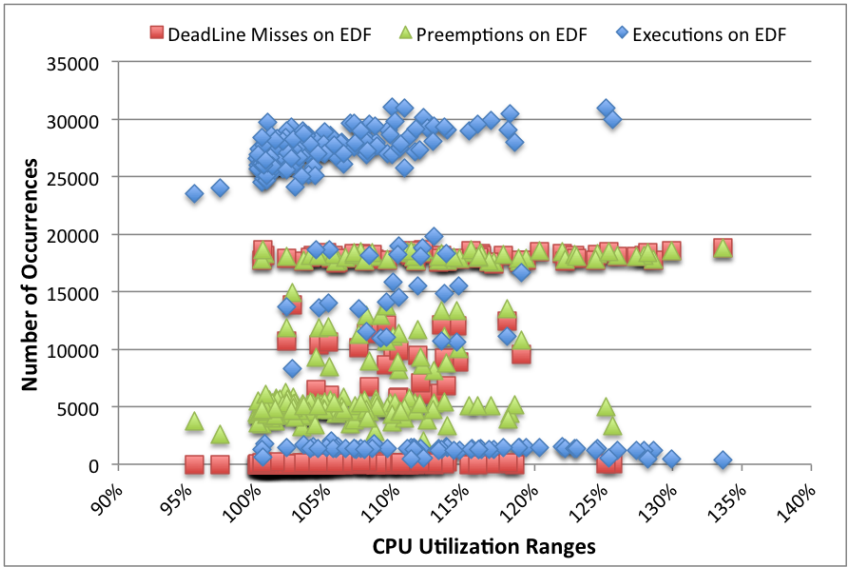

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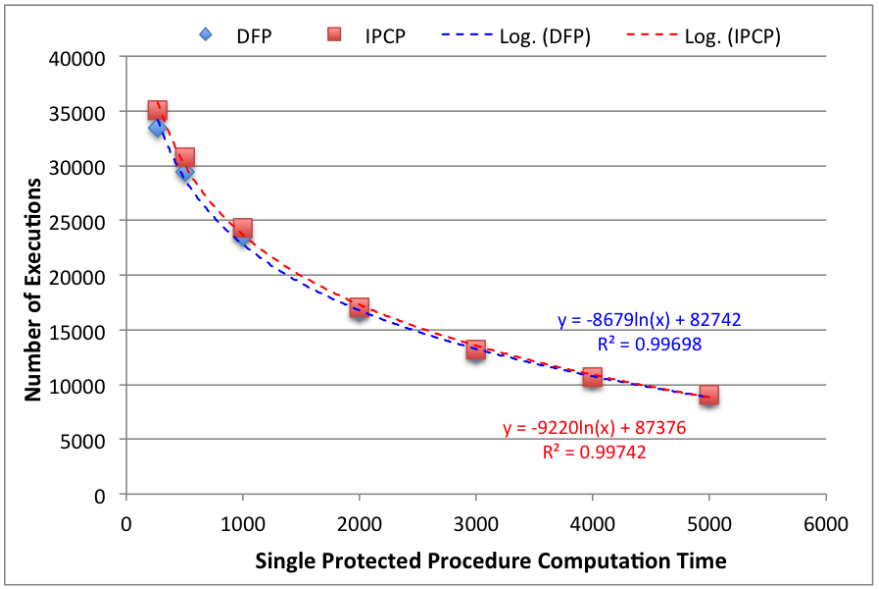

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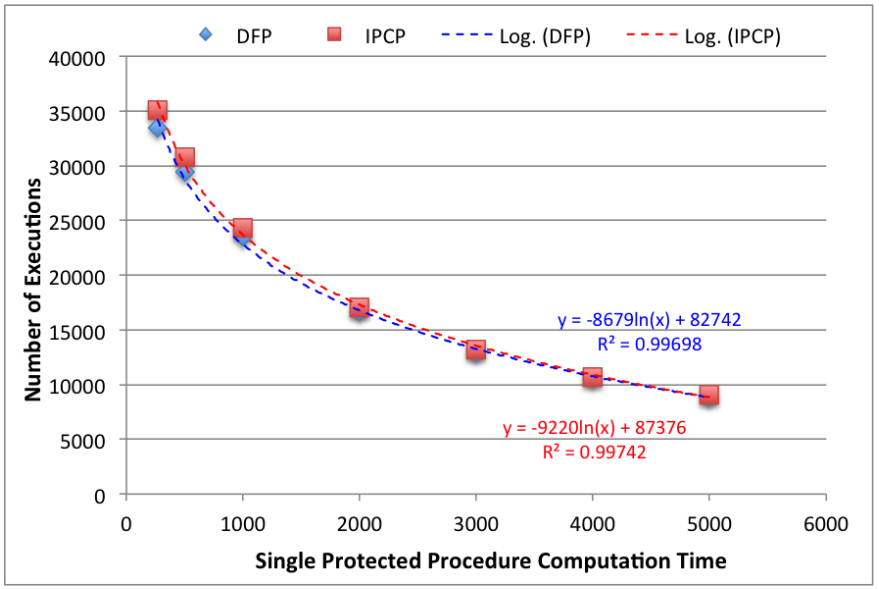

- It presents a logarithmic converging progression as the computation time of the protected procedure increases
- DFP incurs more cumulative overhead than IPCP
  - Due to the need to read the clock in checking absolute deadlines

Is it feasible to migrate Ravenscar-EDF from LEON to ARM technology?

- We analyzed the ARM Cortex-M version of the AdaCore runtime in the GAP-2016 offering

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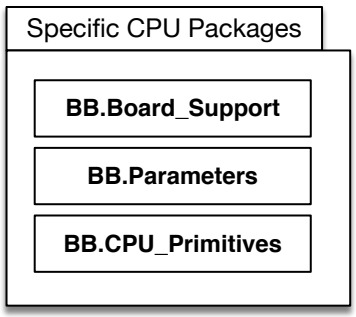

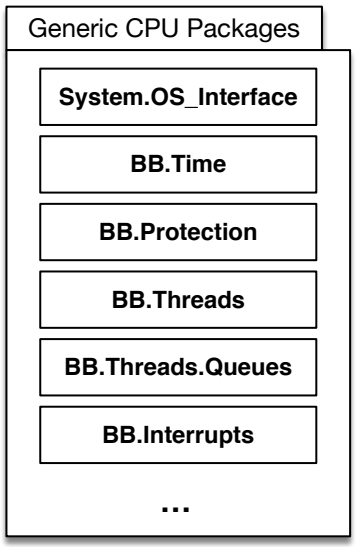

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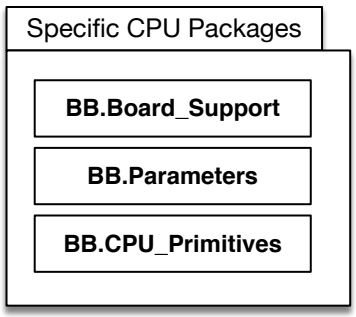

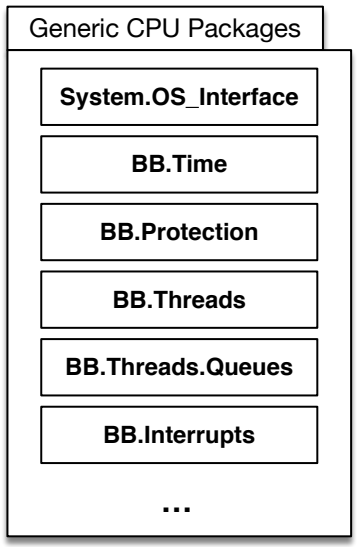

- The FPS version can be easily converted to EDF one modifying only a small part of the original packages
- This should yield a runtime with more widespread use than for the LEON processor family

How can we take benefit of the best of both?

- EDF generates a feasible schedule (if any exists) within 100% CPU utilization
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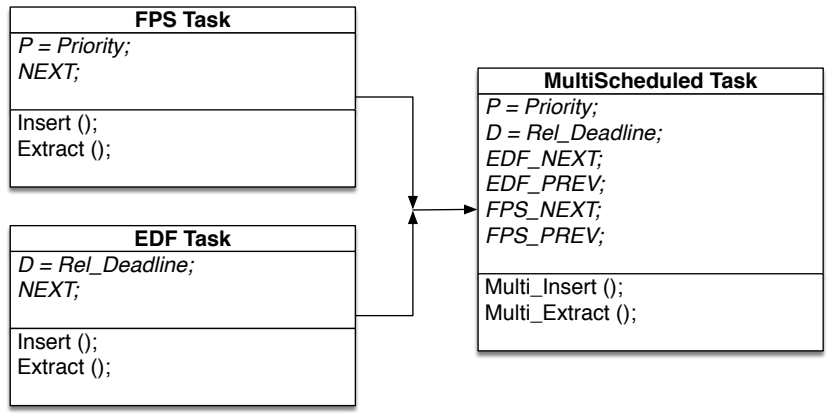
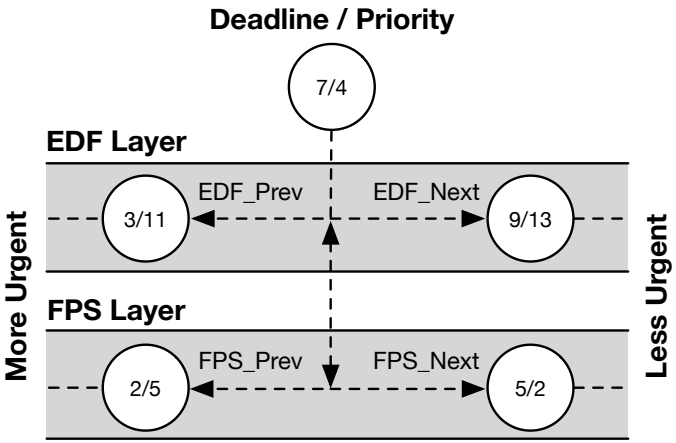
The Solution

A co-existence of both algorithms should yield the best of both worlds: EDF "becomes" FPS above 100% load

- A double linkedlist could offer a quick switch mechanism
- It should be based on a threshold value computed dynamically by the runtime on the idle time



Protocol complexity



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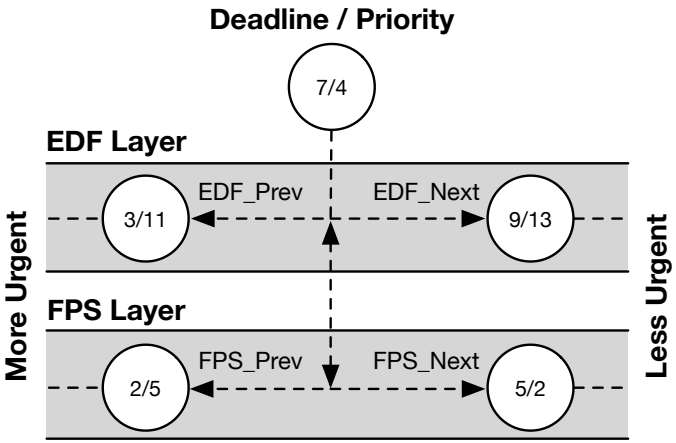

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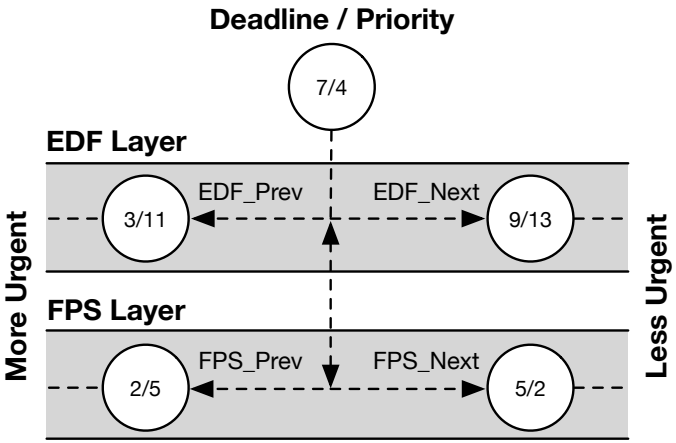

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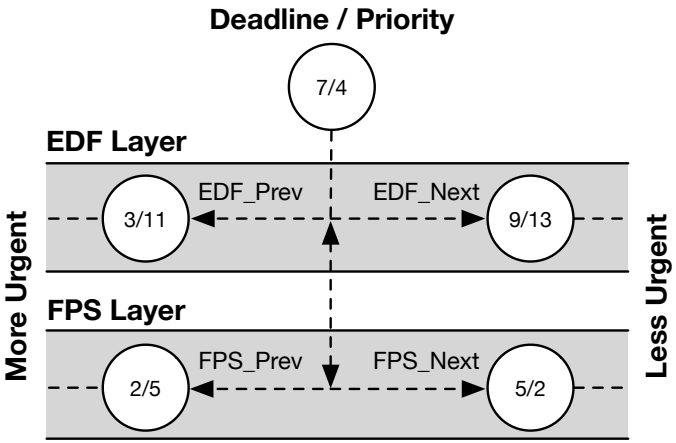

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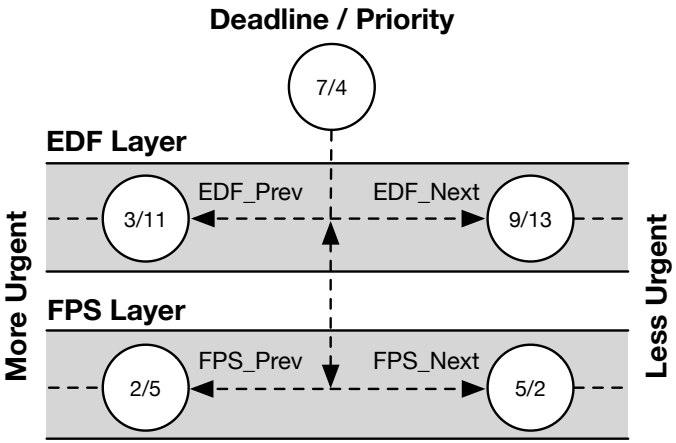

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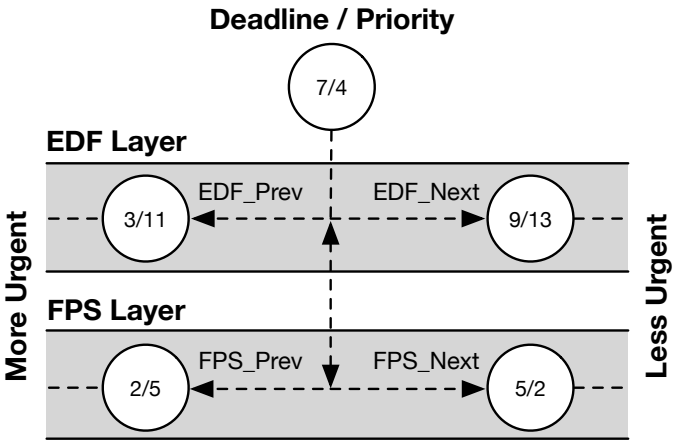

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- Yet, interrupts could be difficult to manage in a dual scheme

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  - We also experimentally observed the fragility of EDF in contrast to the resilience of FPS under overload conditions
- We provided a baseline technology to further investigate this matter
- We are contemplating some hypothesis to combine the best of EDF and FPS in a single runtime